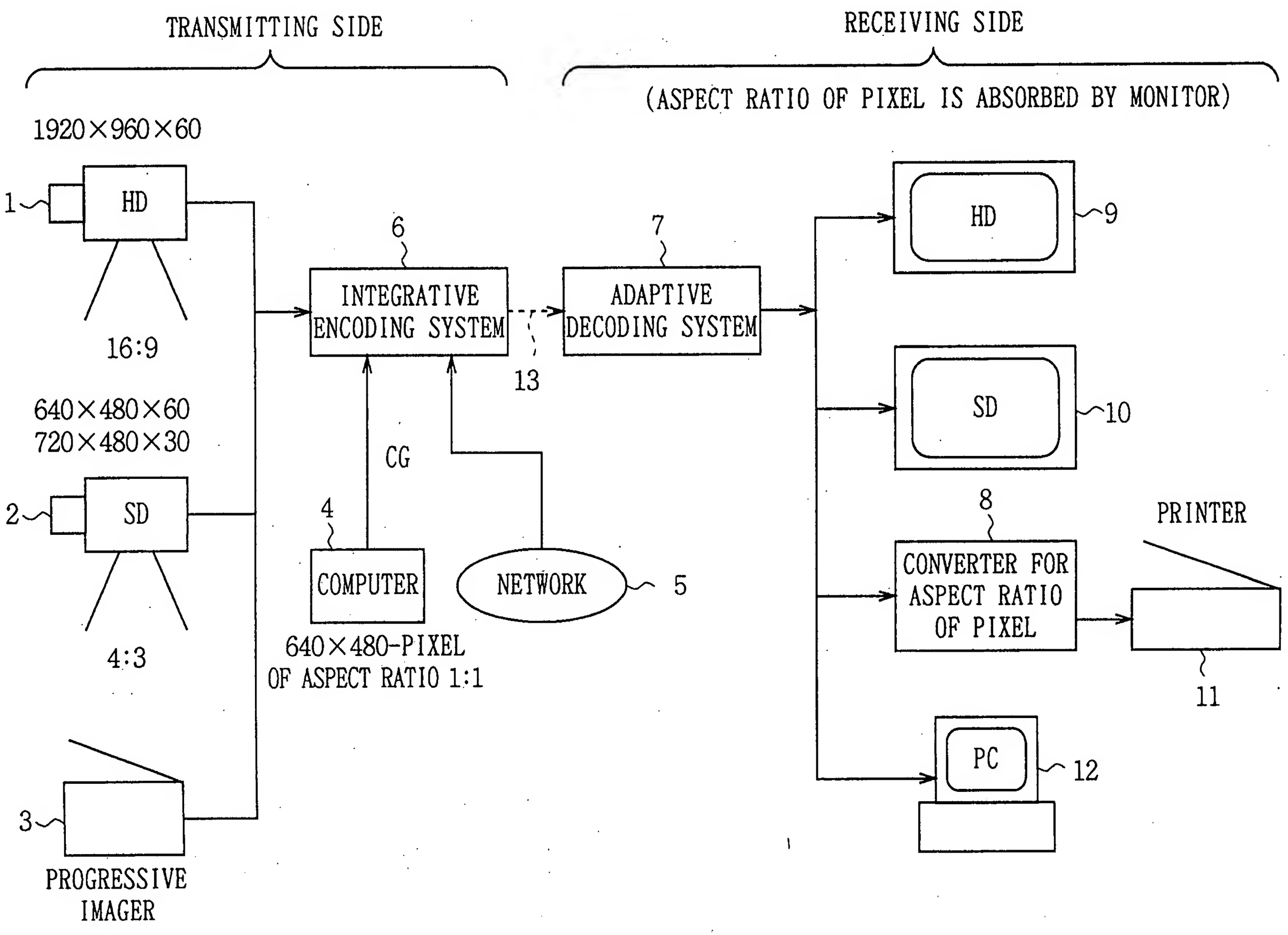
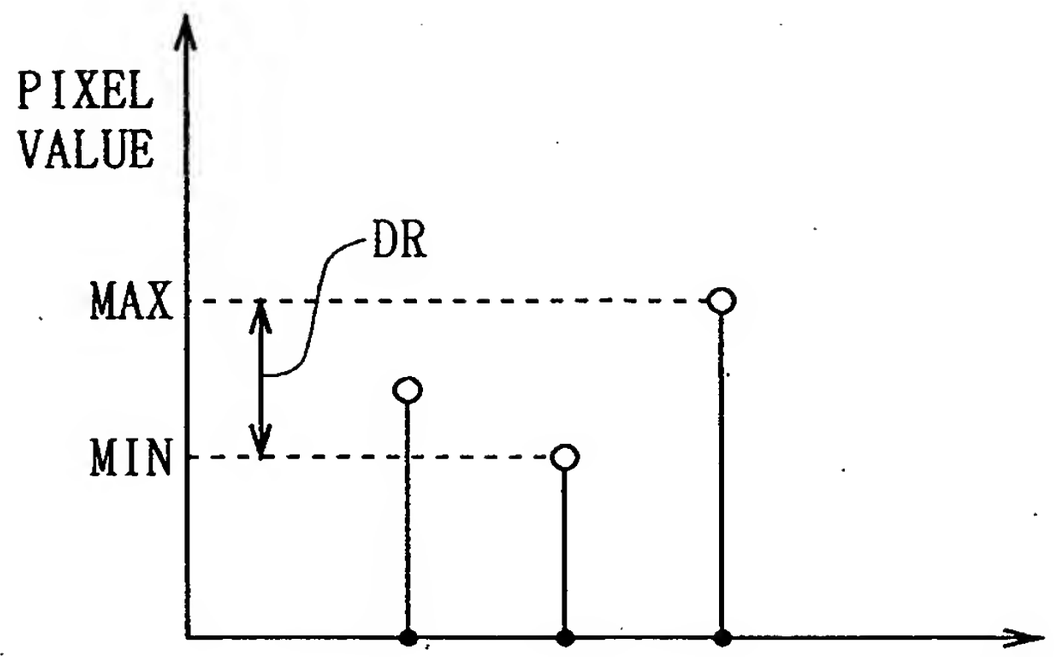
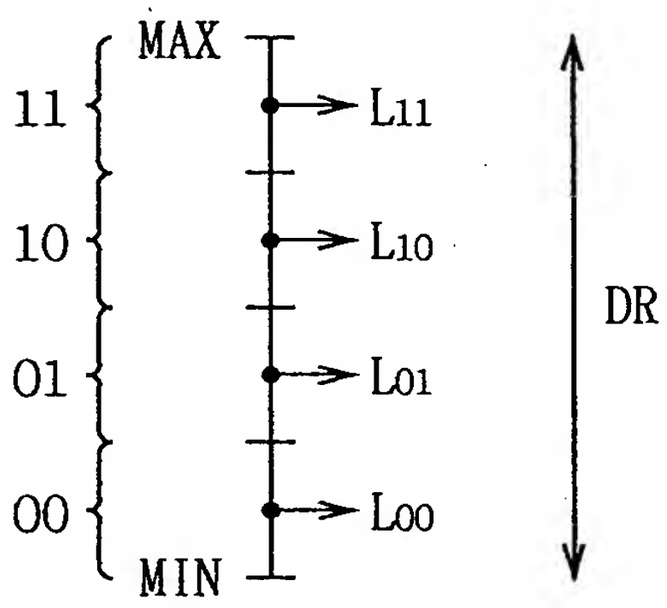

TRANSMITTING SIDE
RECEIVING SIDE
(ASPECT RATIO OF PIXEL IS ABSORBED BY MONITOR)
1920×960×60
1
HD
16:9
640×480×60
720×480×30
2
SD
4:3
3
PROGRESSIVE IMAGER
6
INTEGRATIVE ENCODING SYSTEM
13
7
ADAPTIVE DECODING SYSTEM
CG
4
COMPUTER
640×480-PIXEL OF ASPECT RATIO 1:1
NETWORK
5
HD
9
SD
10
8
CONVERTER FOR ASPECT RATIO OF PIXEL
PRINTER
11
PC
12

FIG. 1

A

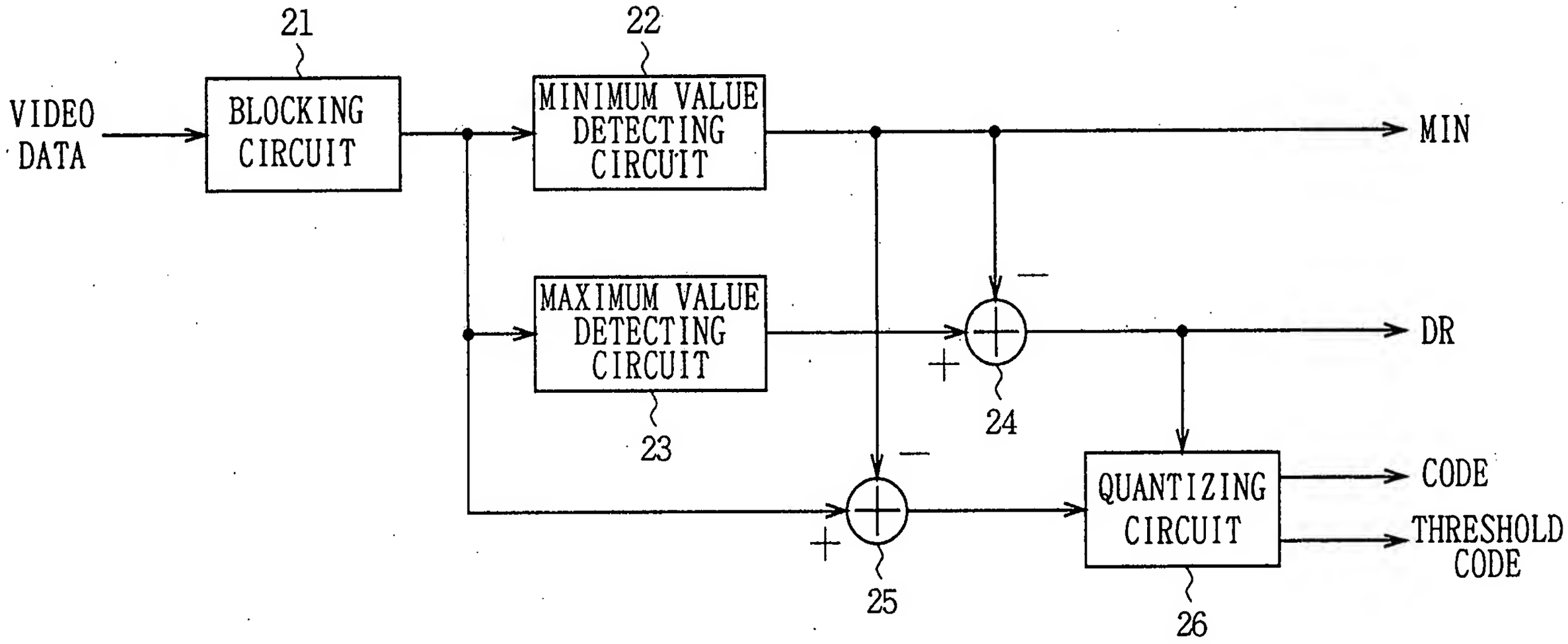


B



ADRC PROCESSING

FIG. 2



ADRC PROCESSING CIRCUIT

FIG. 3

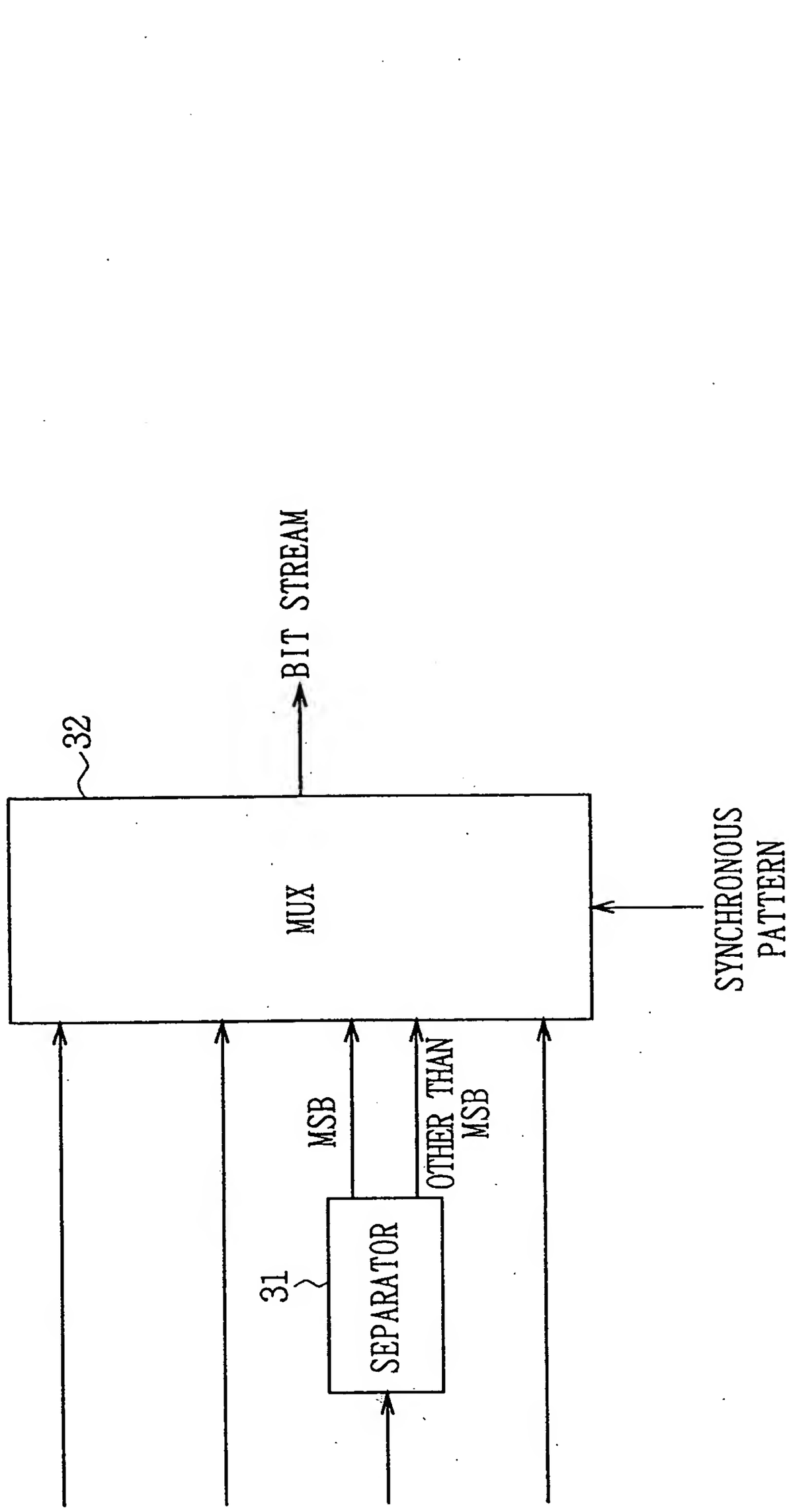

BIT-STREAM FORMING CIRCUIT
SYNCHRONOUS PATTERN
MUX
32
MSB
OTHER THAN MSB
SEPARATOR
31
MIN
DR
CODE
THRESHOLD CODE

FIG. 4

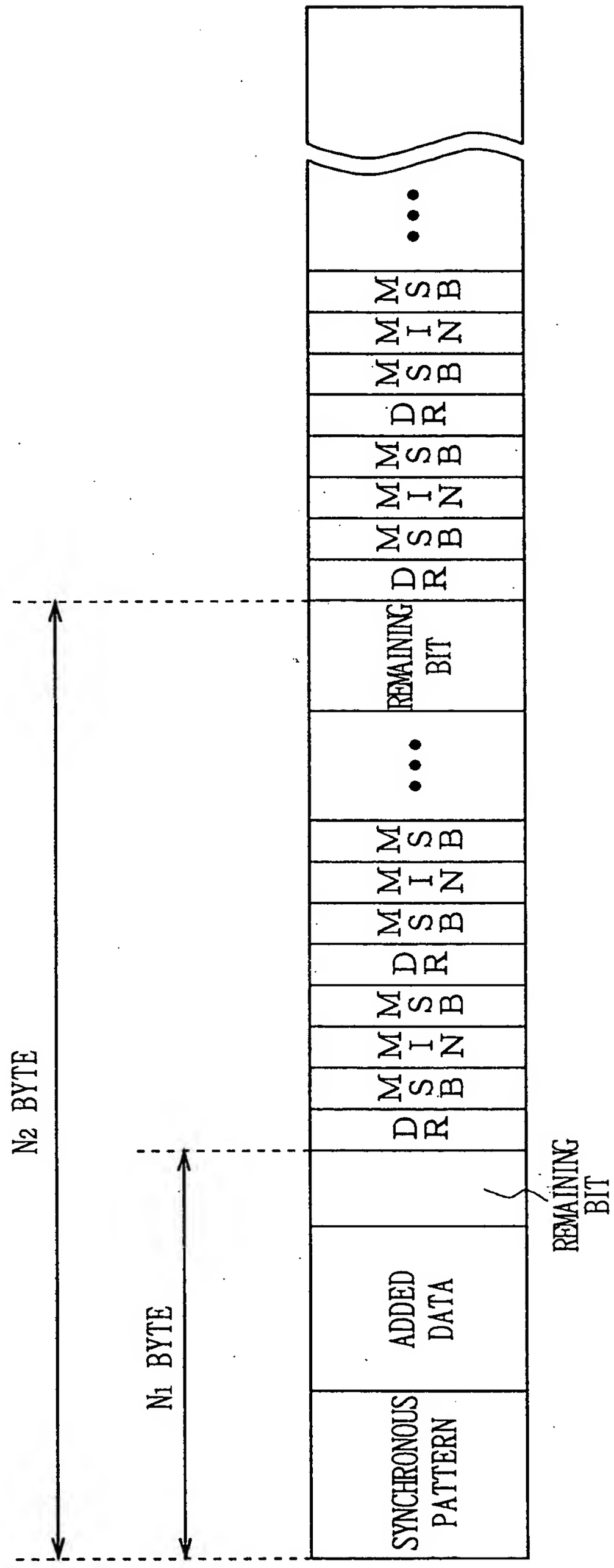

SYNCHRONOUS PATTERN
ADDED DATA
REMAINING BIT
N1 BYTE
N2 BYTE
REMAINING BIT
MSB
MIN
MSB
DR
MSB
MIN
MSB
DR
MSB
MIN
MSB
DR
MSB
MIN
MSB
DR

FIG. 5

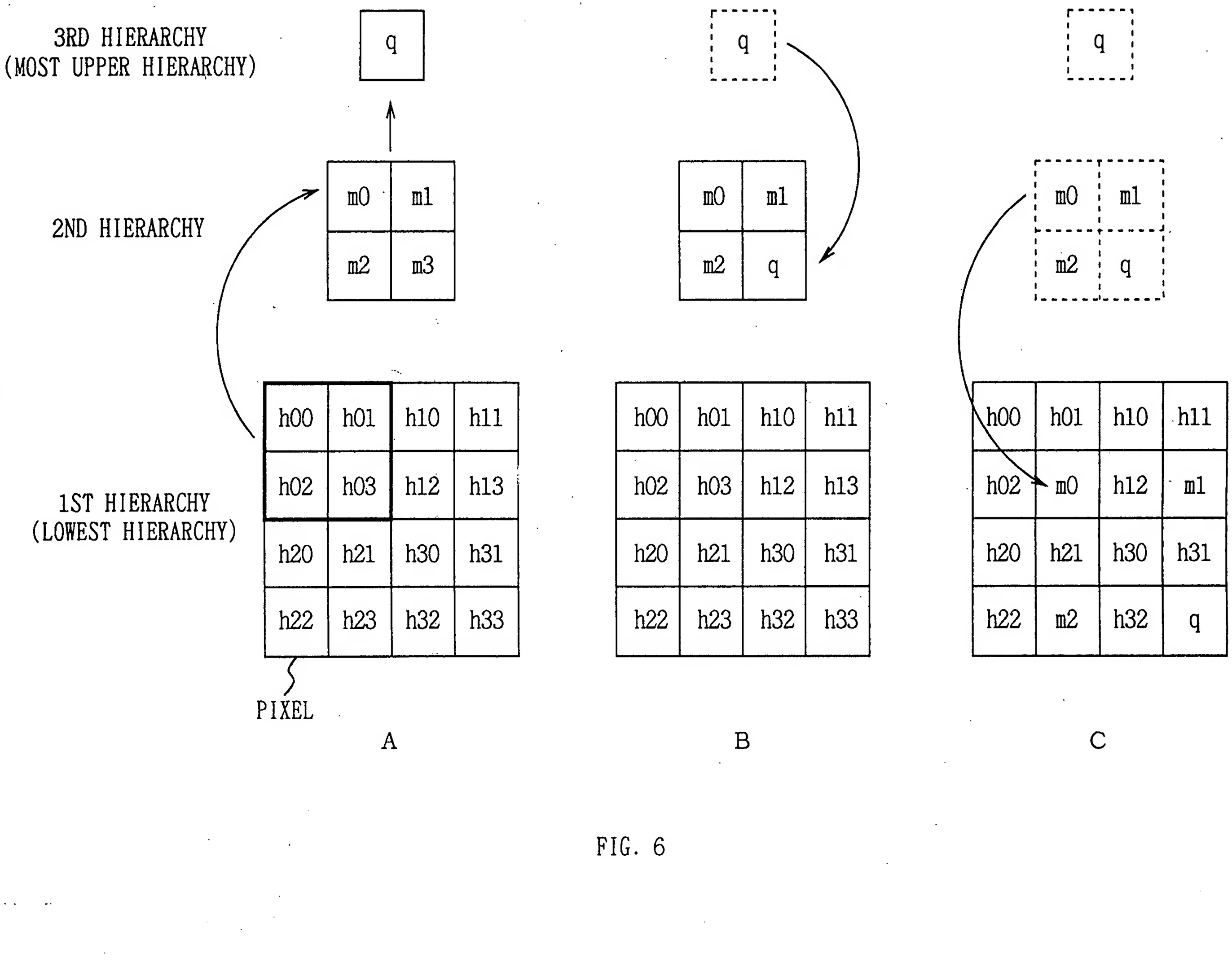
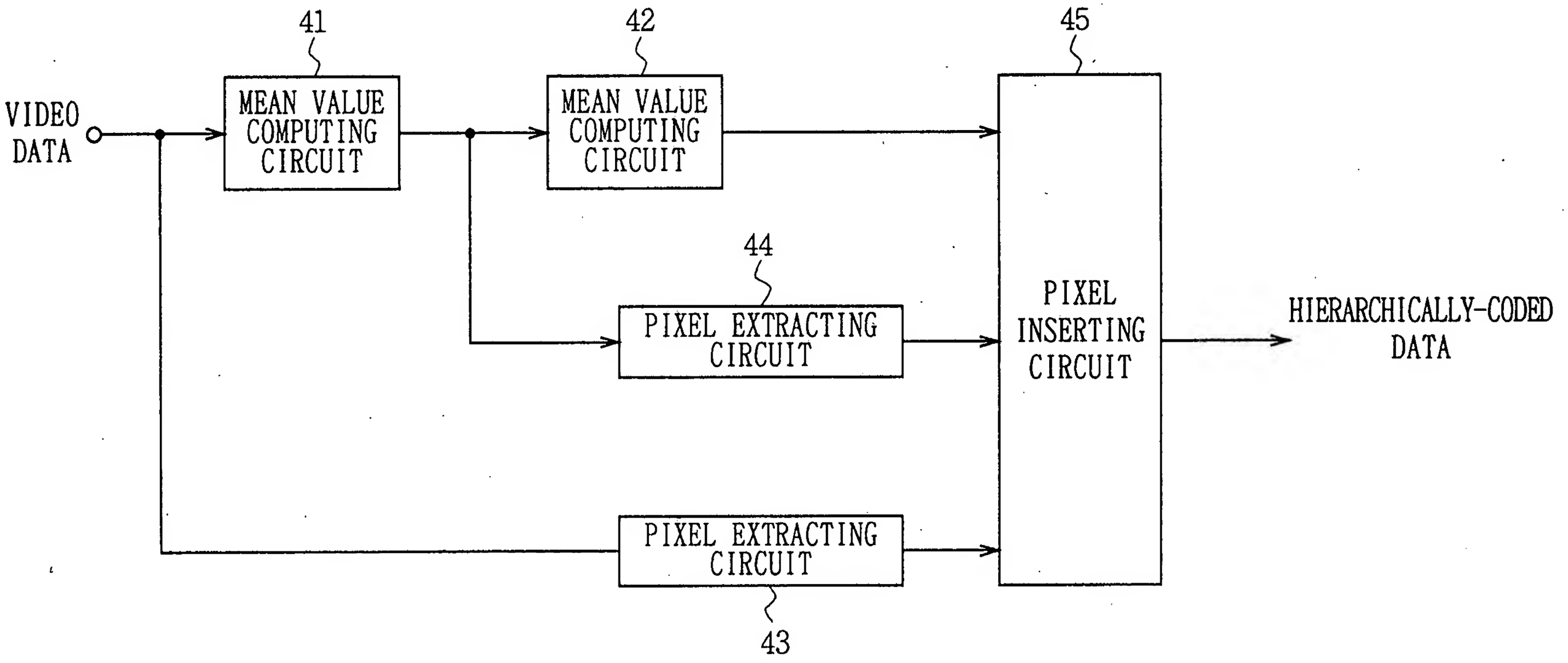

3RD HIERARCHY
(MOST UPPER HIERARCHY)
q
2ND HIERARCHY
m0
m1
m2
m3
1ST HIERARCHY
(LOWEST HIERARCHY)
h00
h01
h10
h11
h02
h03
h12
h13
h20
h21
h30
h31
h22
h23
h32
h33
PIXEL
A
B
C

FIG. 6



HIERARCHICAL ENCODER

FIG. 7

ISDB TRANSMITTER

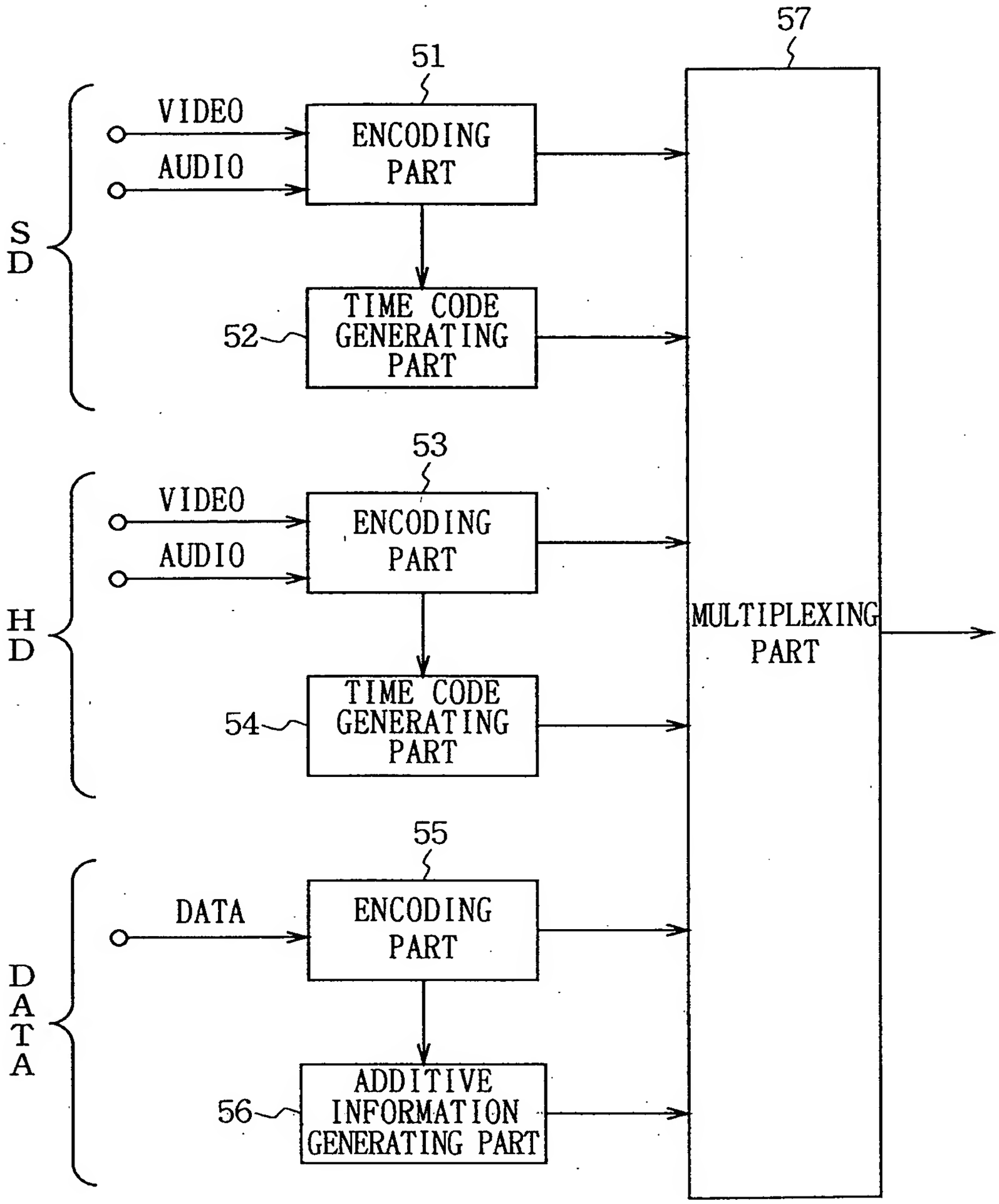
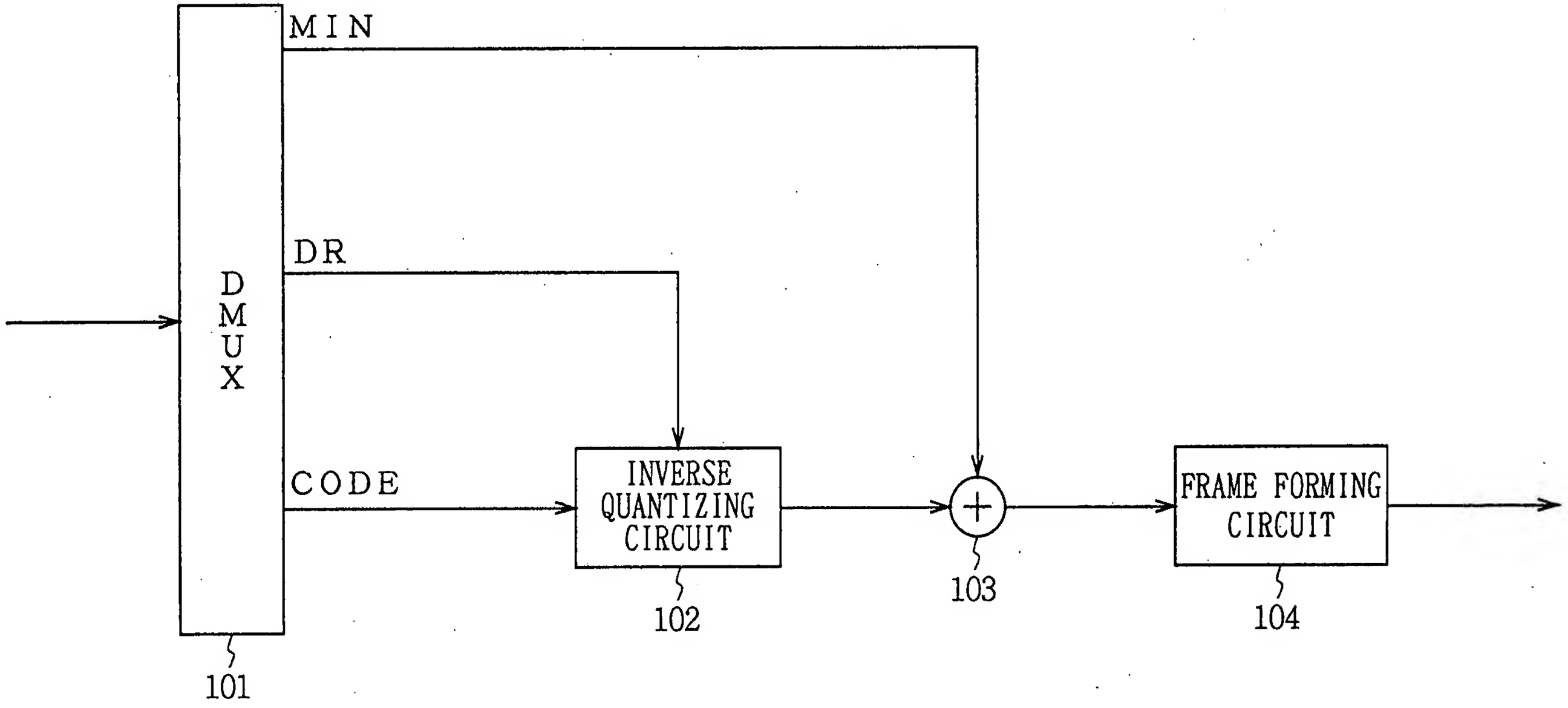
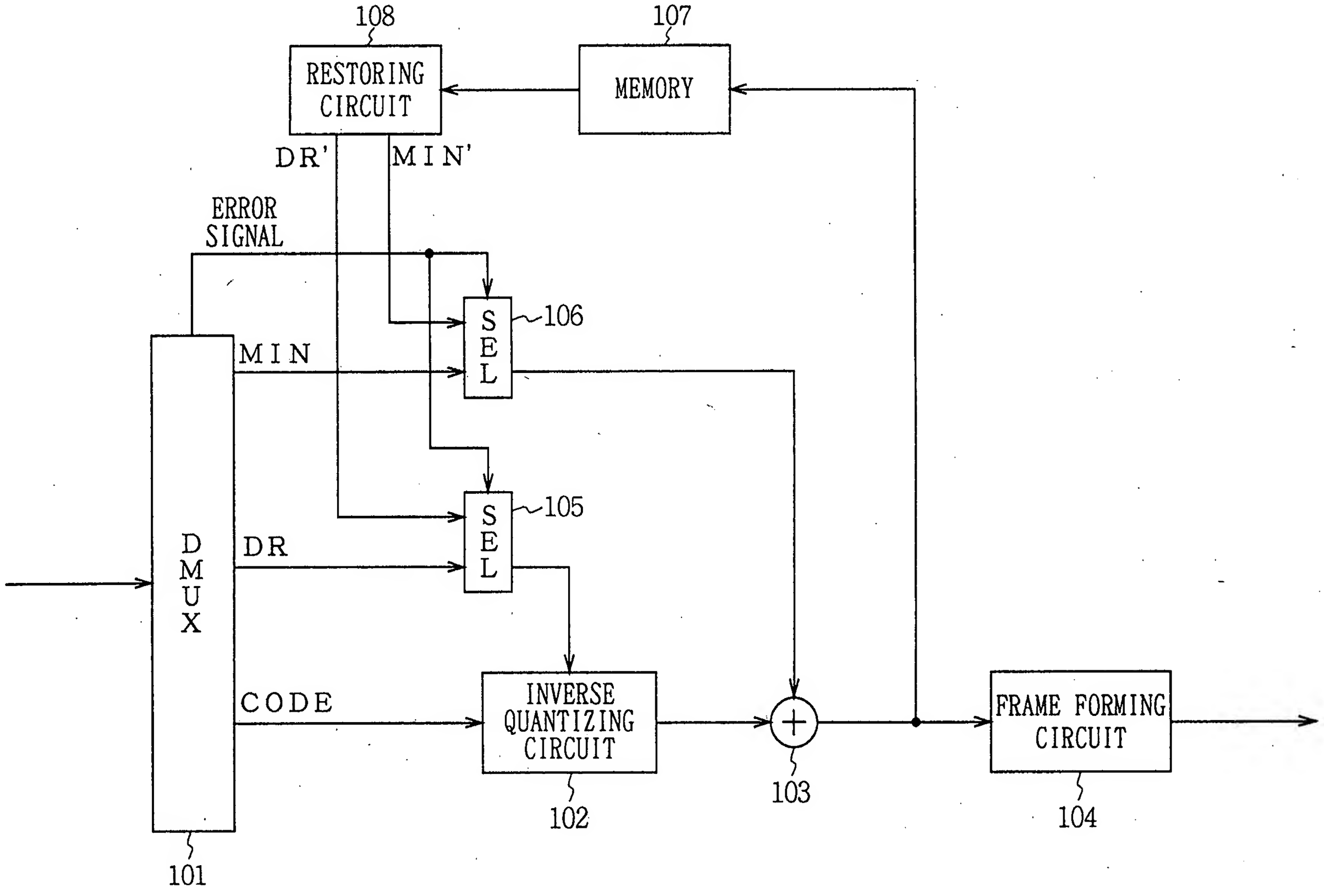


FIG. 8



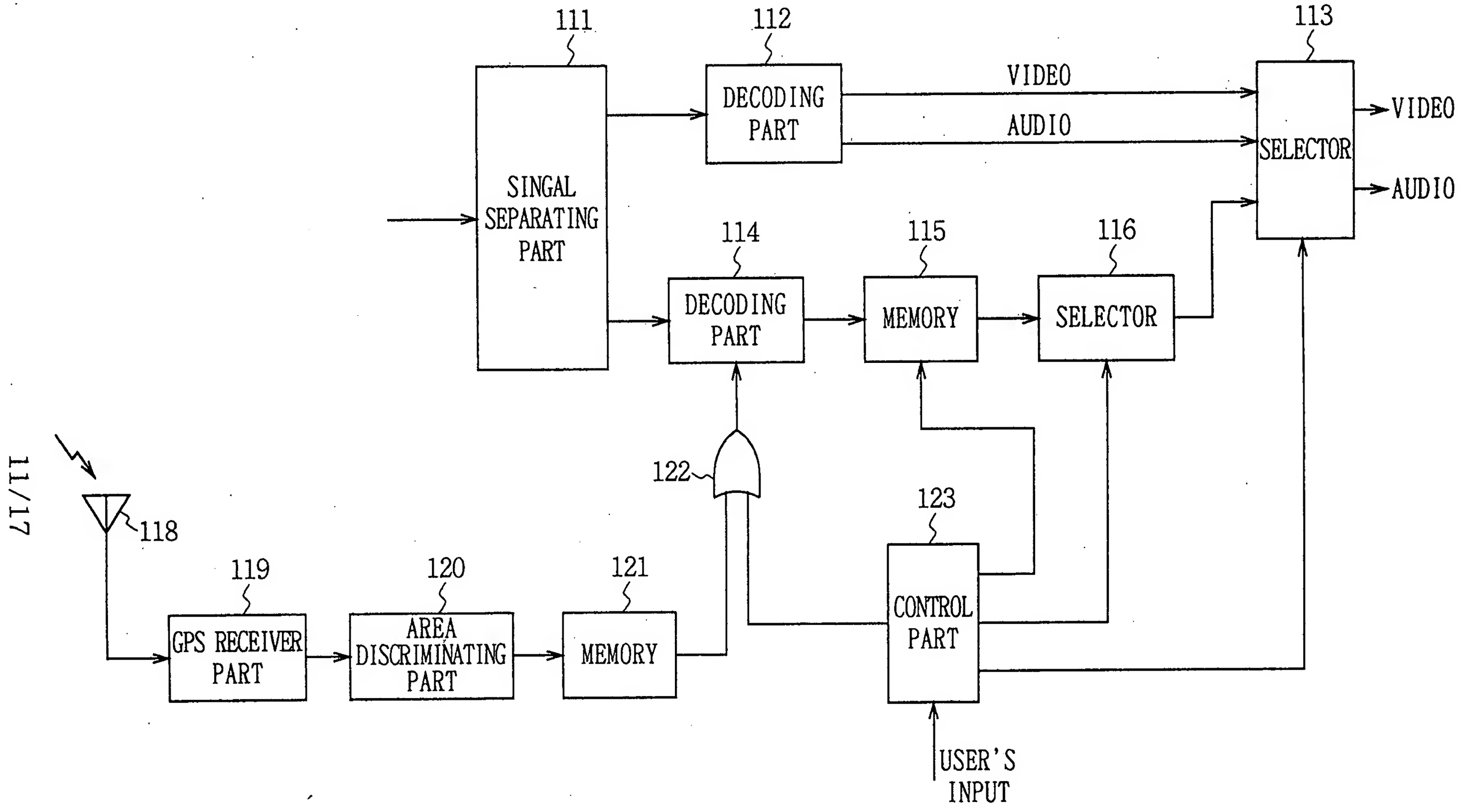
ADRC DECODING CIRCUIT

FIG. 9



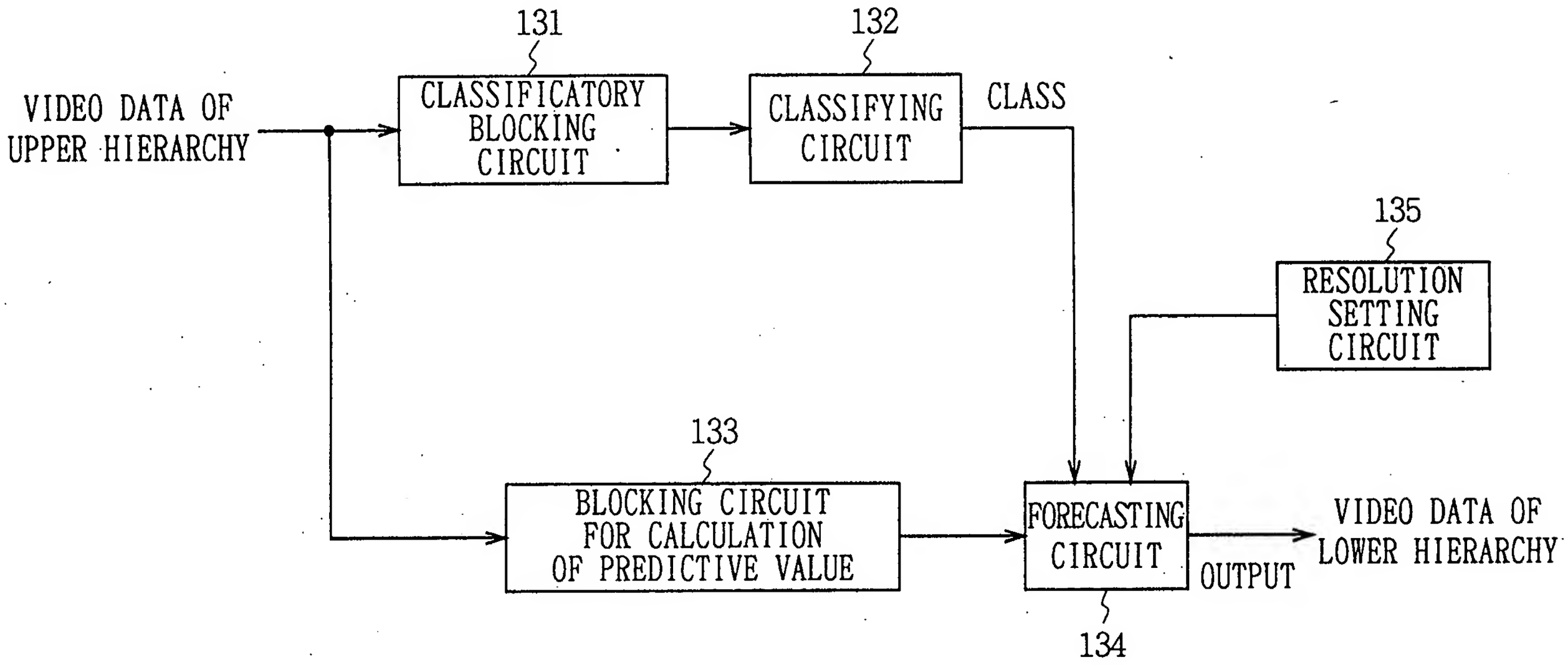
ADRC DECODING CIRCUIT

FIG. 10



ISDB RECEIVER

FIG. 11



RESOLUTION CREATING CIRCUIT

FIG. 12

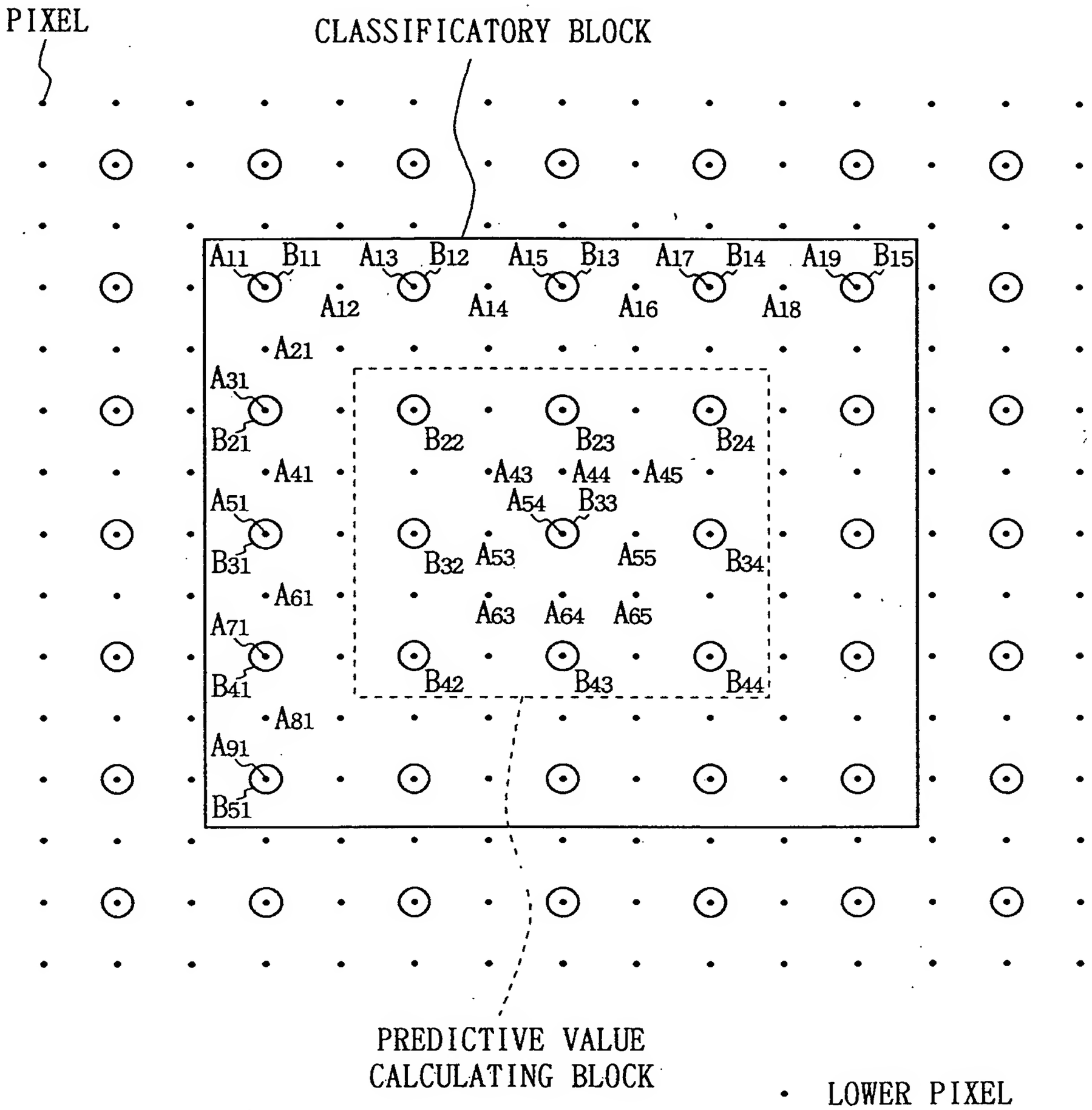

PIXEL
CLASSIFICATORY BLOCK
A11 B11 A13 B12 A15 B13 A17 B14 A19 B15
A12 A14 A16 A18
A21
A31
B21
B22 B23 B24
A41
A43 A44 A45
A51
A54 B33
B31
B32 A53 A55 B34
A61
A63 A64 A65
A71
B41
B42 B43 B44
A81
A91
B51
PREDICTIVE VALUE
CALCULATING BLOCK
• LOWER PIXEL
○ UPPER PIXEL

FIG. 13

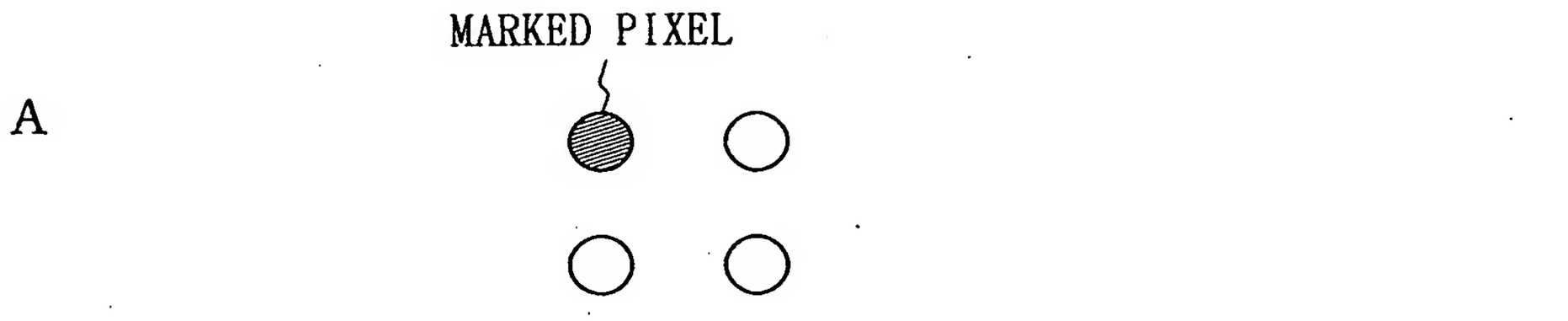


FIG. 14

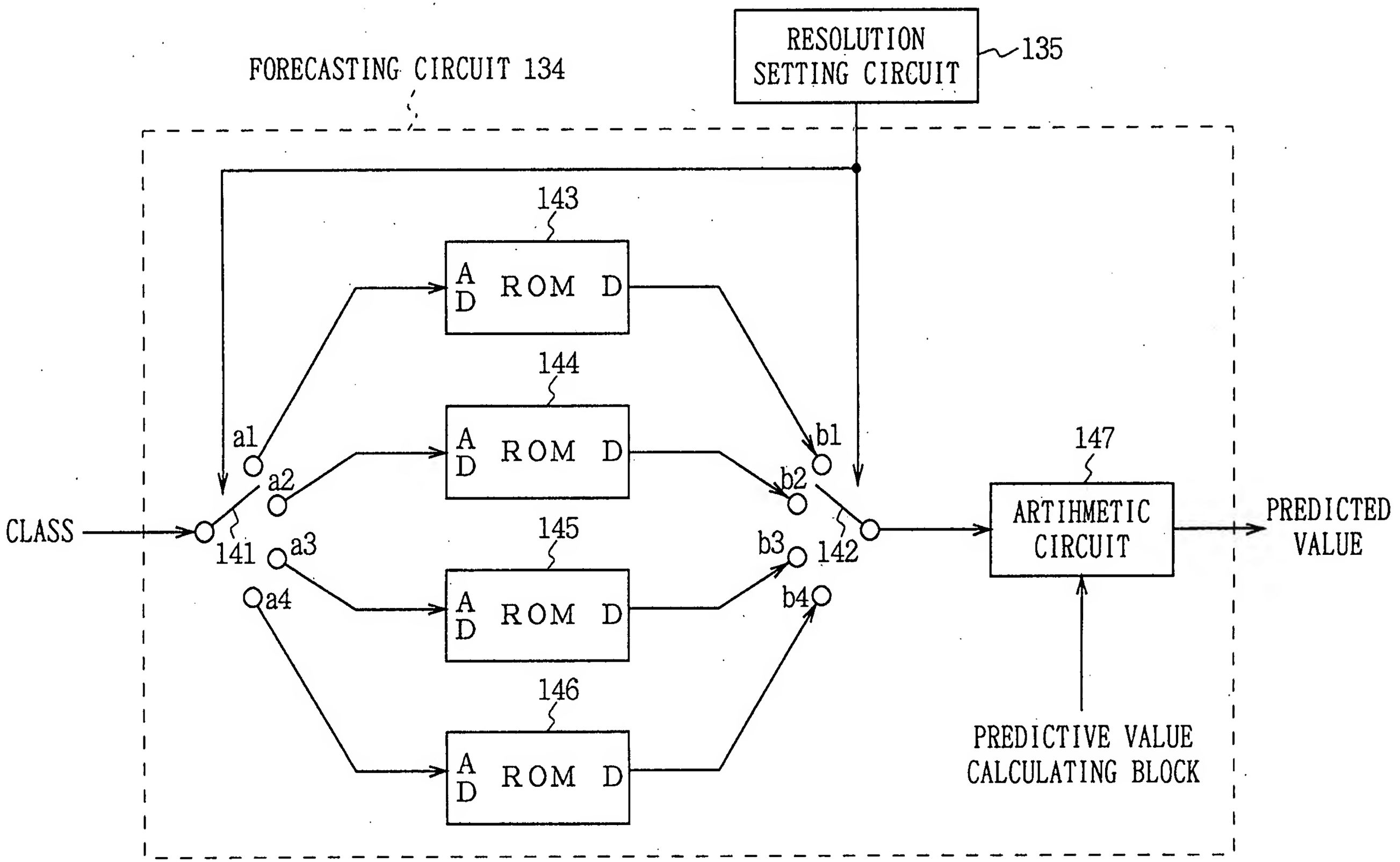

FORECASTING CIRCUIT 134
RESOLUTION SETTING CIRCUIT
135
143
A D ROM D
144
A D ROM D
145
A D ROM D
146
A D ROM D
CLASS
141
a1
a2
a3
a4
b1
b2
b3
b4
142
147
ARTIHMETIC CIRCUIT
PREDICTED VALUE
PREDICTIVE VALUE CALCULATING BLOCK

FIG. 15

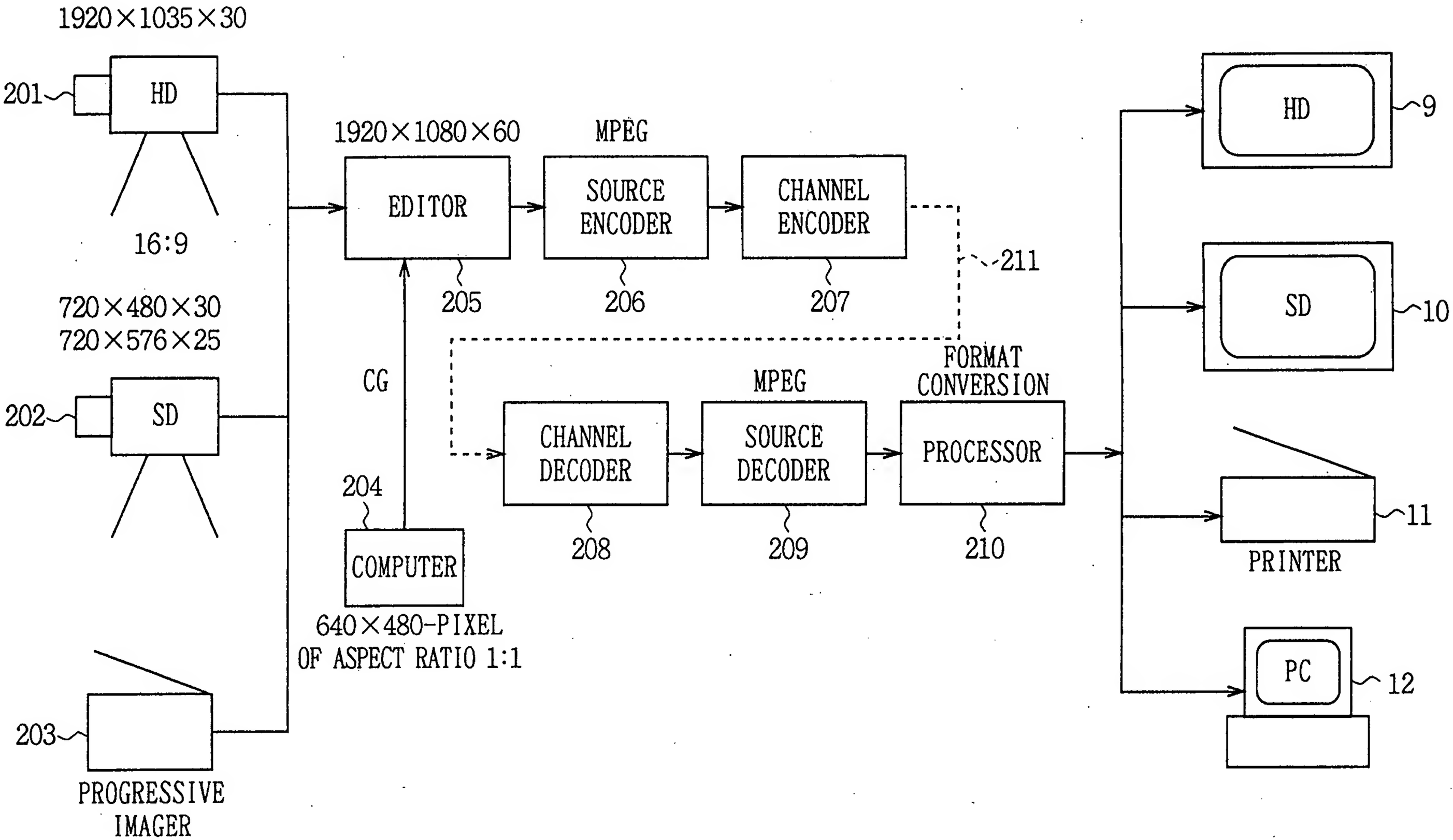

1920×1035×30
201
HD
16:9
720×480×30
720×576×25
202
SD
203
PROGRESSIVE IMAGER
1920×1080×60
MPEG
EDITOR
SOURCE ENCODER
CHANNEL ENCODER
205
206
207
211
CG
204
COMPUTER
640×480-PIXEL OF ASPECT RATIO 1:1
FORMAT CONVERSION
MPEG
CHANNEL DECODER
SOURCE DECODER
PROCESSOR
208
209
210
HD
9
SD
10
11
PRINTER
PC
12

FIG. 16

Explanation of Ref r nc Numerals

1, 2...video camera, 3...progressive imager, 4...computer, 5...network, 6...integrative encoding system, 7...adaptive decoding system, 8...converter for aspect ratio of pixel, 9, 10... display, 11...printer, 12...computer display, 13...transmission line, 21...blocking circuit, 22...minimum value detecting circuit, 23...maximum value detecting circuit, 24, 25...computing unit, 26...quantizing circuit, 31...separator, 32...multiplexer, 41, 42...mean value computing circuit, 43, 44...pixel extracting circuit, 45...pixel inserting circuit, 51...encoding part, 52... time code generating part, 53...encoding part, 54...time code generating part, 55...encoding part, 56...additive information generating part, 57...multiplexing part, 101...demultiplexer, 102...inverse quantizing circuit, 103...arithmetic unit, 104... frame forming circuit, 105,106...selector, 107...memory, 108... restoring circuit, 111...signal separating part, 112...decoding part, 113...selector, 114...decoding part, 115...memory, 116... selector, 118...antenna, 119...GPS receiver part, 120...area discriminating part, 121...memory, 122...OR gate, 123...control part, 131...classificatory blocking circuit, 132...classifying circuit, 133...blocking circuit for calculation of predictive value, 134...forecasting circuit, 135...resolution setting circuit, 141, 142...switch, 143 - 146...ROM, 147...arithmetic circuit.

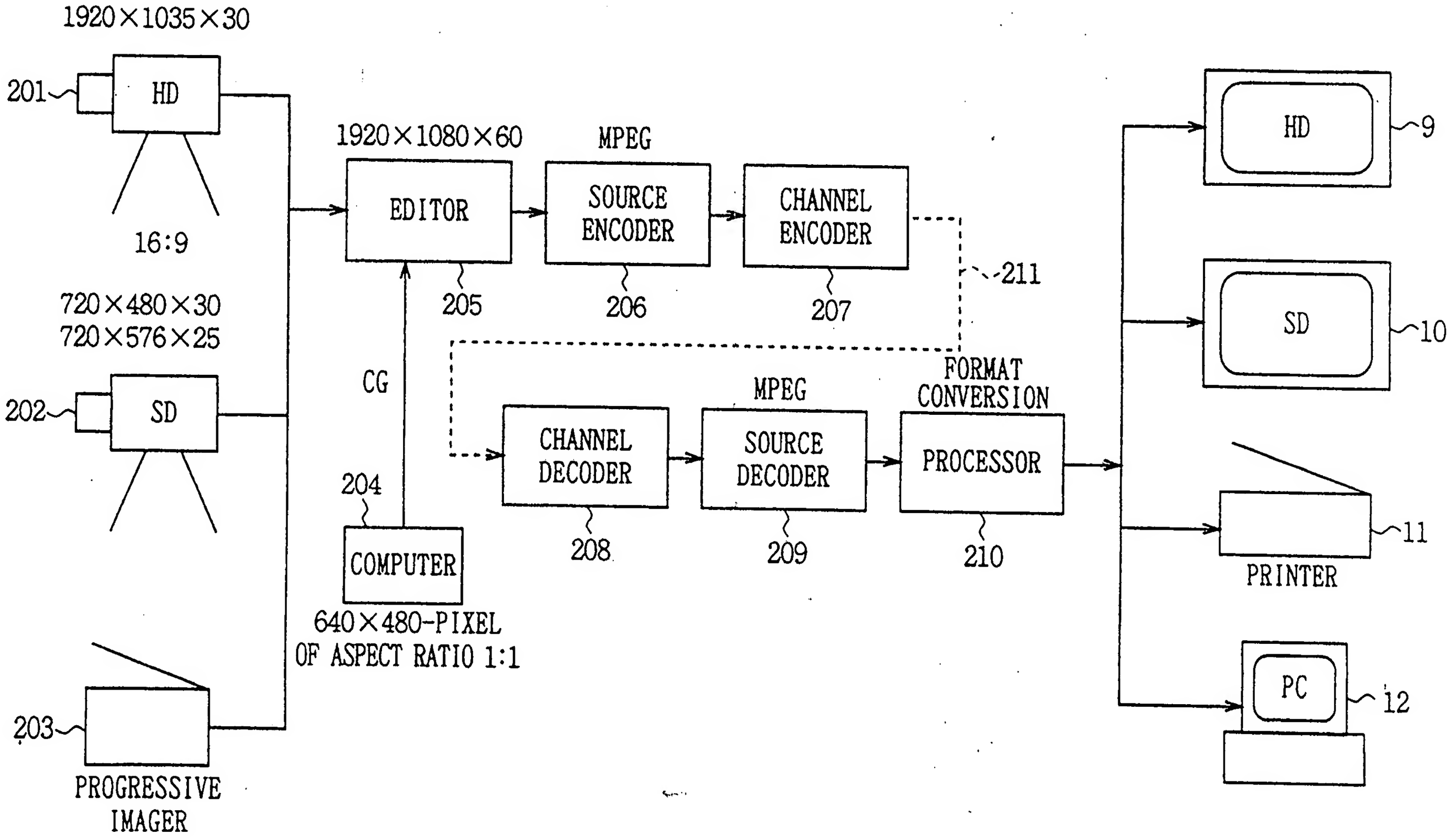


FIG. 16

(RELATED ART)